DHCAL Back-End

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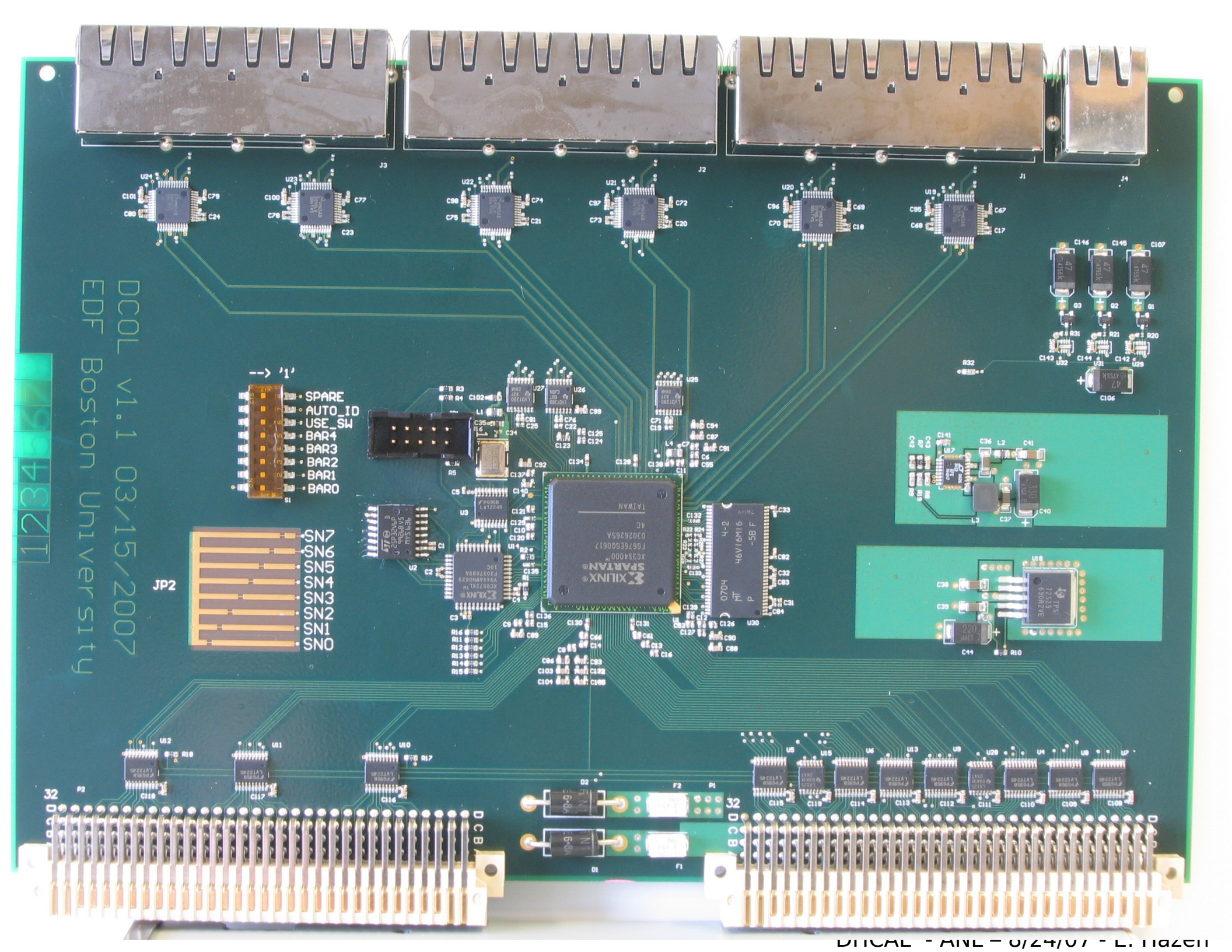
DCOL Status

- DCOL Worked (as far as we know!) for the TB effort
- To go forward for m^3 effort:
  - Hardware:
    - Produce 12-15 more boards
    - Front panels
    - Any other anticipated changes?
  - Firmware (preliminary list, please add):
    - Review buffering scheme
    - Define error bits, add error counters
    - Provide simple way to clear memory
    - Modify checksum definition to ease software checking

DCOL Firmware

- Review of buffering scheme
  - Is circular buffer mode good enough, or do we need a paged mode of some sort?
  - Is timestamp sorting needed?
    - If so, we need a documented upper limit on buffering latency in front-end
  - Perhaps a dedicated meeting/teleconference should be held to discuss this?
- Any other issues?



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